iSBX 328™ ANALOG OUTPUT MULTIMODULE™ BOARD HARDWARE REFERENCE MANUAL

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Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

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PREFACE

This manual provides general information, preparation for use, programming information, principles of operation, and service information for the iSBX 328 Analog Output Multimodule Board. Supplementary information is provided in the following documents.

- Intel MCS-85 User's Manual, Order No. 9800366.
- Intel Peripheral Design Handbook, Order No. 9800676.
- Intel Multibus Specification, Order No. 9800683.
- Intel iSBX Bus Specification, Order No. 142686.
- Intel MCS-48 and UPI-41 Assembly Language Manual, Order No. 9800255.
- Intel UPI-41 Assembly Language Reference Card, Order No. 9800871.

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ILLUSTRATIONS

CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBX 328 Analog Output Multimodule Board is a member of Intel's growing family of expansion boards designed to allow quick, easy, and inexpensive expansion capability for the Intel single board computer product line. The iSBX 328 Analog Output Multimodule Board (hereafter referred to as the Multimodule board) provides the ability to add analog output capability to any host iSBC microcomputer that contains an iSBX bus connector. This manual contains the information required to use the Multimodule board, including chapters on general information, preparation for use, programming, principles of operation, and service information.

1-2. DESCRIPTION

The Multimodule board, shown in figure 1-1, is designed to plug onto any host iSBC microcomputer that contains an iSBX bus connector. The board uses an 8041 UPI device to control eight analog output channels that may be user-configured via jumpers to operate in bipolar voltage output mode (-5 to +5 volts), unipolar voltage output mode (0 to +5 volts), or current loop output mode (4 to 20 mA) applications. Channels may be individually wired for simultaneous operation in both current loop output and voltage output applications. The outputs from 50-pin edge connector J1 on the Multimodule board are pin-compatible with the iCS 910 Signal Conditioning/Termination Panel.

All data to be output through the Multimodule board is transferred from the host iSBC microcomputer to the Multimodule board via the iSBX bus connector (P1). The UPI device on the Multimodule board accepts the binary digital data and generates a 12-bit data word for the Digital-to-Analog Converter (DAC) and a four bit channel decode/enable for selecting the output channel. The DAC transforms the data into analog signal outputs for either voltage output mode or current loop output mode. Offsetting of the DAC voltage in current output mode may be performed by the UPI software offset routine or by the hardware offset adjustments included on the board. The Multimodule board status is available via the iSBX bus connector (P1).

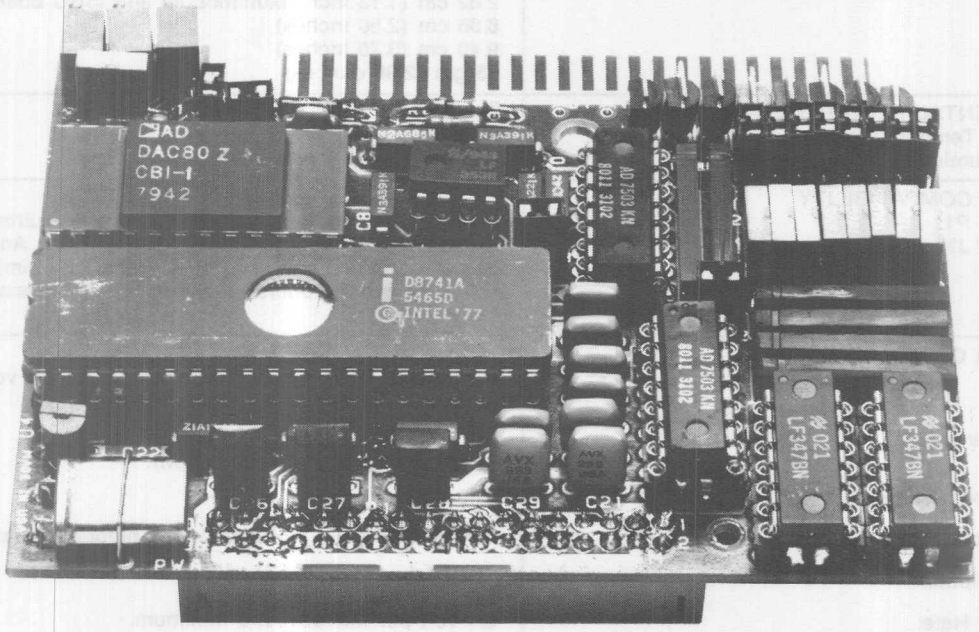


Figure 1-1. iSBX 328™ Analog Output Multimodule™ Board

1-3. EQUIPMENT SUPPLIED

The Multimodule board plugs directly onto the host iSBX microcomputer, thereby requiring no cable interface. The following equipment is supplied with the iSBX 328 Analog Output Multimodule Board:

a. Schematic Diagram, drawing number 142760.
b. Two plastic mounting screws, 1/4 6-32.
c. One Plastic mounting spacer, 1/2 6-32.

1-4. COMPATIBLE EQUIPMENT

The Multimodule board must be used with a host iSBC microcomputer that contains an iSBX bus connector. Multibus interfacing is performed indirectly through the host iSBC microcomputer.

The output connector (J1) on the Multimodule board interfaces readily to an iCS 910 Analog Signal Conditioning/Termination Panel through the J2 connector on the panel. Although the outputs are not pin-for-pin compatible, the Multimodule board can be installed into most analog output applications satisfied by an iSBC 724 or 732 board.

1-5. SPECIFICATIONS

The specifications for the iSBX 328 Analog Output Multimodule Board are listed in table 1-1.

Table 1-1. Specifications

POWER REQUIREMENTS	
Vcc ± +5 volts (±0.25 volts)	Icc = 140 mA maximum
Vdd ± +12 volts (±0.6 volts)	Idd = 45 mA (Voltage Mode) Idd = 200 mA (Current Loop Mode, if iSBX 328 Vdd is used)
Vss = -12 volts (±0.6 volts)	Iss = 60 mA maximum
PHYSICAL CHARACTERISTICS	
Height:	2.03 cm (0.80 inch) Multimodule board. 2.82 cm (1.13 inch) Multimodule and iSBC boards.
Width:	6.36 cm (2.50 inches)
Length:	9.40 cm (3.70 inches)
Weight:	85 gm (2.98 ounces)
ENVIRONMENTAL REQUIREMENTS	
Operating Temperature:	0° to 55°C (32° to 131°F)
Relative Humidity:	To 90% (without condensation)
INTERFACE COMPATIBILITY	
Connector P1: Connector J1:	Compatible with the iSBX bus interface requirements. Analog pin-out compatible with the ICS 910 Analog Signal Conditioning/Termination Panel and similar to the iSBC 724 and 732 boards. Connector details are contained in table 2-5.
OPERATING CHARACTERISTICS	
Outputs:	8 channels, each independently jumpered for voltage output or current loop output mode.
Voltage Ranges:	0 to +5 volts (unipolar operation). -5 to +5 volts (bipolar operation).
Current Loop Range:	4 to 20 mA.
Output Current:	±5 mA maximum (voltage mode—bipolar operation).
DAC Resolution:	12 bits.
DAC Slew Rate:	0.1 volt per microsecond minimum.
DAC Throughput Rate:	1 channel operation = 5 kHz. 8 channel operation = 800 Hz.

Table 1-1. Specifications (Continued)

DAC Accuracy:
(%FSR / C)

Mode	Accuracy	Ambient Temp
Voltage—Unipolar, typical	±0.025% FSR	@ 25°C
Voltage—Unipolar, maximum	±0.035% FSR	@ 25°C
Voltage—Unipolar, typical	±0.08% FSR	@ 0° to 60°C*
Voltage—Unipolar, maximum	±0.17% FSR	@ 0° to 60°C*
Voltage—Bipolar, typical	±0.025% FSR	@ 25°C
Voltage—Bipolar, maximum	±0.035% FSR	@ 25°C
Voltage—Bipolar, typical	±0.09% FSR	@ 0° to 60°C*
Voltage—Bipolar, maximum	±0.17% FSR	@ 0° to 60°C*
Current Loop, typical	±0.07% FSR	@ 25°C
Current Loop, maximum	±0.08%, FSR	@ 25°C
Current Loop, typical	±0.17% FSR	@ 0° to 60°C
Current Loop, maximum	±0.37% FSR	@ 0° to 60°C

* (At = 35°C)

Temperature Coefficient:

Mode	Gain TC	Offset TC
Voltage—Unipolar, typical	16 ppm	06 ppm
Voltage—Unipolar, maximum	33 ppm	17 ppm
Voltage—Bipolar, typical	16 ppm	08 ppm
Voltage—Bipolar, maximum	33 ppm	15 ppm
Current Loop, typical	43 ppm	07 ppm
Current Loop, maximum	87 ppm	18 ppm

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter of the text provides information on preparing and installing the iSBX 328 Analog Output Multimodule Board. The information presented in this chapter includes unpacking and inspection instructions; installation considerations such as physical, power, cooling, and mounting requirements; dc characteristics; connector assignments; jumper configuration; and installation procedures.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and the packing material for the agent's inspection.

For repair to a product damaged in shipment, contact the Intel Product Service Hotline to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that the salvageable shipping cartons and packing material be saved for future use in the event that the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

Installation considerations such as power cooling, mounting, and physical size requirements, are outlined in the following paragraphs.

NOTE

If modification of the Multimodule board is required, ensure that none of the iSBX bus specifications or standards are violated.

2-4. POWER REQUIREMENTS

The Multimodule board requires three voltages for operation; +5 volts (±0.25 volt) at 140 mA maximum, -12 volts (±0.6 volt) at 60 mA maximum, and +12 volts (±0.6 volt) at 45 mA maximum (200 mA maximum current for a current loop application when the iSBX 328 board power is used). All power for the Multimodule board is drawn through the iSBX bus connector (P1) on the board.

The Multimodule board uses the -12 volt power provided through the iSBX bus connector and components R7 and VR1 to create a -6.4 volt reference for use with the analog circuitry. A reference voltage of +6.3 volts is generated within the DAC.

2-5. COOLING REQUIREMENTS

The Multimodule board dissipates 27.9 gram-calories/minute (0.11 BTU/minute) of heat and adequate circulation of air must be provided to prevent a temperature rise above 55°C (134°F).

2-6. MOUNTING REQUIREMENTS

Figure 2-1 shows the Multimodule board and the location of the iSBX bus connector and the mounting hole. The Multimodule board mounts onto any host iSBC microcomputer containing an iSBX bus connector and the required mounting hole. The mounting hardware supplied with the Multimodule board includes:

a. 2 plastic screws, 1/4 inch 6-32, separate from board.

b. 1 plastic spacer, 1/2 inch 6-32, separate from board.

c. 36-pin connector P1, factory installed onto board.

NOTE

The Multimodule board, when installed onto a host iSBC microcomputer, occupies an additional card slot within an iSBC 604/614 Cardcage and adjacent to the component side of the host iSBC microcomputer.

2-7. PHYSICAL DIMENSIONS

The outside dimensions of the Multimodule board are as follows:

a. Width: 6.35 cm (2.50 inches).
b. Length: 9.40 cm (3.70 inches).
c. Height: 1.40 cm (0.56 inch) Multimodule board only.
2.82 cm (1.13 inches) Multimodule and iSBC boards.

Figure 2-1 shows the outside dimensions of the board and figure 2-2 gives the maximum height dimensions for the Multimodule board mounted onto a host iSBC microcomputer.

2-8. DC INTERFACE CHARACTERISTICS

The dc characteristics of the iSBX 328 Analog Output Multimodule Board at the P1 connector are listed in table 2-1.

2-9. JUMPER CONFIGURATIONS

The iSBX 328 Analog Output Multimodule Board contains 36 jumper pads which perform the functions as outlined in table 2-2 and detailed in the following paragraphs. Table 2-2 also lists the configuration of the board as shipped from the factory; bipolar voltage output mode.

The user-configured jumpers on the Multimodule board include jumpers to select one of four possible operating modes for the board. The board configured for unipolar (0 to +5 volts) voltage output mode operation is shown in figure 2-3. The as-shipped jumper configuration required for bipolar (-5 to +5 volts) voltage output mode operation is shown in figure 2-4. The jumper configuration for current loop output mode operation with hardware-generated current offset is shown in figure 2-5. The jumper configuration for current loop output mode operation with firmware-generated offset and bipolar DAC operation is shown in figure 2-6. Finally, the jumper configuration for current loop output mode operation with firmware-generated offset and unipolar DAC operation is shown in figure 2-7.

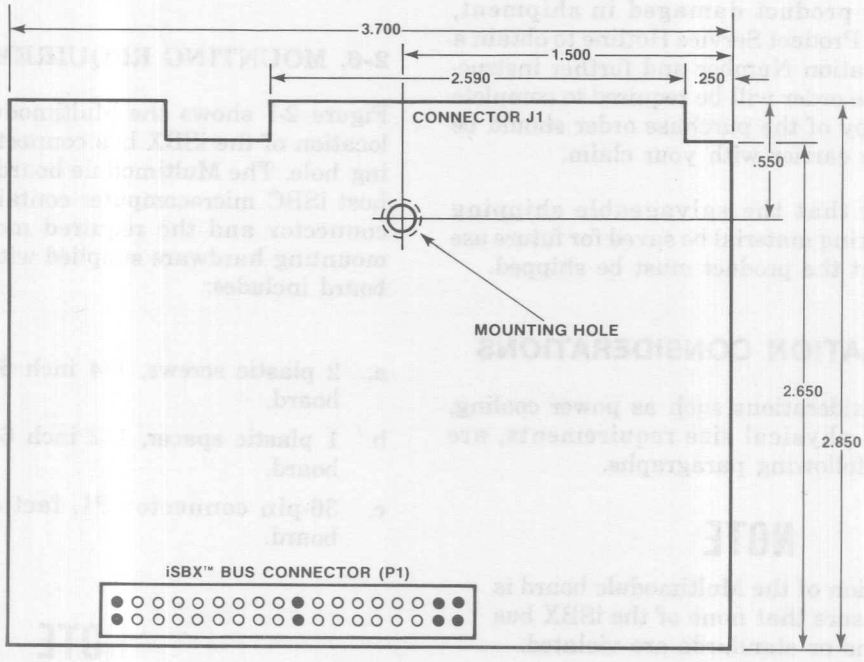


Figure 2-1. Board Dimensions (Inches)

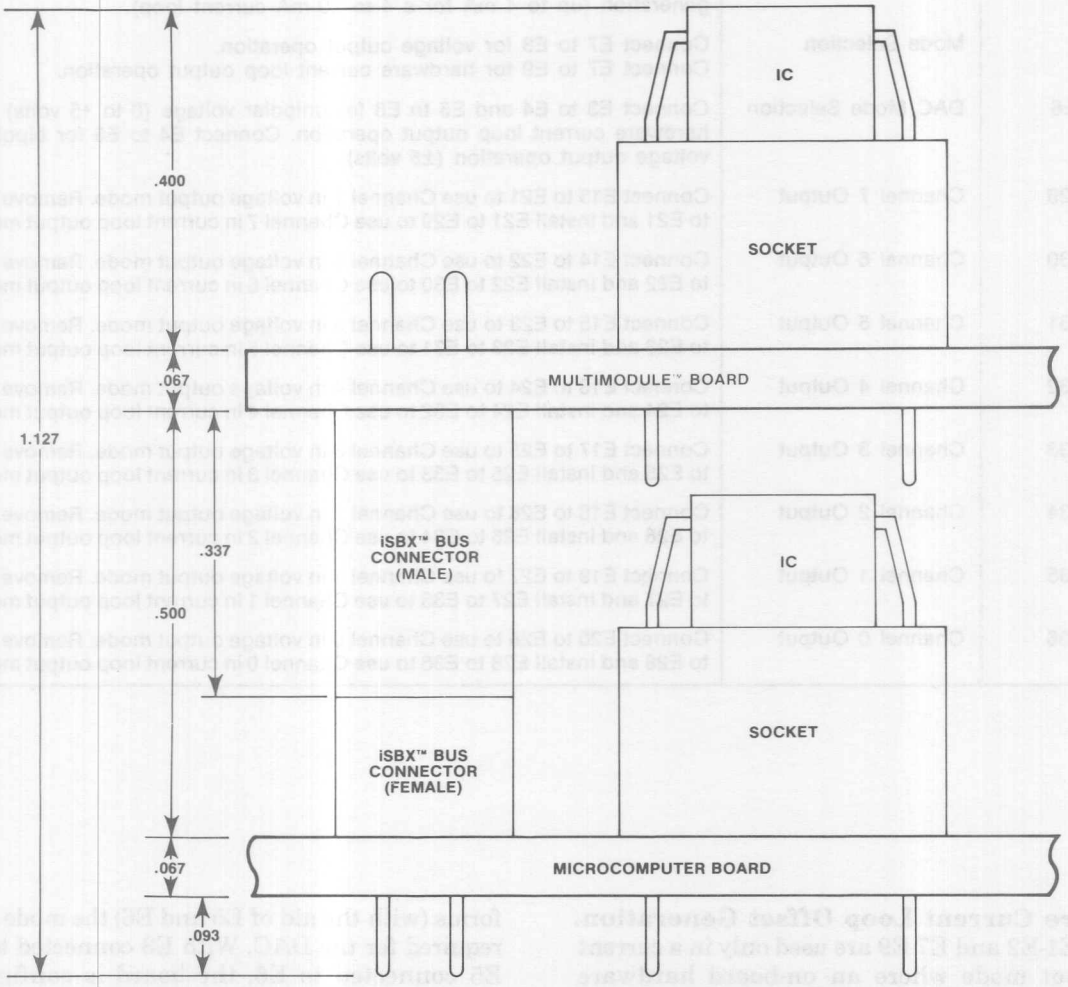


Figure 2-2. Mounting Clearances (Inches)

Table 2-1. DC Interface Characteristics

Output Signal	Type Driver	I_{OL} MAX (mA)	V_{OL} MAX (I_{OL} = MAX)	I_{OH} MIN (μA)	V_{OH} MIN I_{OH} = MIN)	C_O MIN (pf)
MD0-MD7	TRI	2.0	0.45	-400	2.4	130
Input Signal	**Type Receiver**	**I_{IL} MIN (V_{IL} = 0.4)**	**V_{IL} MAX**	**I_{IH} MAX (V_{IH} = 2.4)**	**V_{IH} MAX**	**C_I MAX (pf)**
MD0-MD7	TRI	-0.01	0.8	10	2.0	12
MA0	TTL	-0.01	0.8	10	2.0	10
MCS0/	TTL	-0.01	0.8	10	2.0	10
MRESET	descrete	-1.5	0.4	1	*5.0	10
IOWRT/, IORD/	TTL	-0.01	0.8	10	2.0	10

TTL = Standard Totem Pole Output
TRI =Three-State Output
*Indicates that a pull-up resistor is required for the transistor.

Table 2-2. User-Configurable Jumpers

Jumper Numbers	Functions	Comments
E1,E2	Hardware Configured	Connection of E1 to E2 allows on-board control of the offset current generation (up to 4 mA for a 4 to 20 mA current loop).
E7,E8,E9	Mode Selection	Connect E7 to E8 for voltage output operation. Connect E7 to E9 for hardware current loop output operation.
E3,E4,E5,E6	DAC Mode Selection	Connect E3 to E4 and E5 to E6 for unipolar voltage (0 to +5 volts) and hardware current loop output operation. Connect E4 to E5 for bipolar voltage output operation (±5 volts).
E13,E21,E29	Channel 7 Output	Connect E13 to E21 to use Channel 7 in voltage output mode. Remove E13 to E21 and install E21 to E29 to use Channel 7 in current loop output mode.
E14,E22,E30	Channel 6 Output	Connect E14 to E22 to use Channel 6 in voltage output mode. Remove E14 to E22 and install E22 to E30 to use Channel 6 in current loop output mode.
E15,E23,E31	Channel 5 Output	Connect E15 to E23 to use Channel 5 in voltage output mode. Remove E15 to E23 and install E23 to E31 to use Channel 5 in current loop output mode.
E16,E24,E32	Channel 4 Output	Connect E16 to E24 to use Channel 4 in voltage output mode. Remove E16 to E24 and install E24 to E32 to use Channel 4 in current loop output mode.
E17,E25,E33	Channel 3 Output	Connect E17 to E25 to use Channel 3 in voltage output mode. Remove E17 to E25 and install E25 to E33 to use Channel 3 in current loop output mode.
E18,E26,E34	Channel 2 Output	Connect E18 to E26 to use Channel 2 in voltage output mode. Remove E18 to E26 and install E26 to E34 to use Channel 2 in current loop output mode.
E19,E27,E35	Channel 1 Output	Connect E19 to E27 to use Channel 1 in voltage output mode. Remove E19 to E27 and install E27 to E35 to use Channel 1 in current loop output mode.
E20,E28,E36	Channel 0 Output	Connect E20 to E28 to use Channel 0 in voltage output mode. Remove E20 to E28 and install E28 to E36 to use Channel 0 in current loop output mode.

Hardware Current Loop Offset Generation. Jumpers E1-E2 and E7-E9 are used only in a current loop output mode where an on-board hardware generated offset must be provided to amplifier U2. When E1 is connected to E2, the 4 mA offset current is user-adjustable via variable resistor R3. The jumper is not required if operating in a voltage output mode or if generating offset via software. The jumper connecting E7 to E9 serves to scale the DAC voltage plus any offset voltage for a 4 to 20mA current range.

NOTE

Current offset may be generated by the software on the host iSBC microcomputer before the data is transferred to the Multimodule board or by the firmware located within the 8041 UPI device on the Multimodule board.

DAC Mode Configuration. Jumpers E3 and E4 control the amount of feedback resistance inserted into the feedback loop between the DAC and amplifier U2 on the Multimodule board, and performs (with the aid of E5 and E6) the mode selection required for the DAC. With E3 connected to E4 and E5 connected to E6, the board is configured for unipolar voltage output mode operation; i.e., analog output from the DAC is within the range of 0 to +5 volts. By connecting the jumper from E5 to E6 when the board is configured to the unipolar mode (0 to +5 volts), a ground is provided to pin 17 of the DAC to maintain a constant current flow through the DAC.

Bipolar configuration of the Multimodule board is performed by removing the jumpers connecting E3 to E4 and E5 to E6, and installing a jumper connecting E4 to E5, which provides a half scale offset. In a bipolar voltage output mode, the DAC produces analog channel output in a -5 to +5 volt range.

Multiplexer Select. Jumper pads E10, E11, and E12 are used to select the type of multiplexer to be installed onto the board at chip locations U3 and U5. This jumper is factory configured and should not be modified.

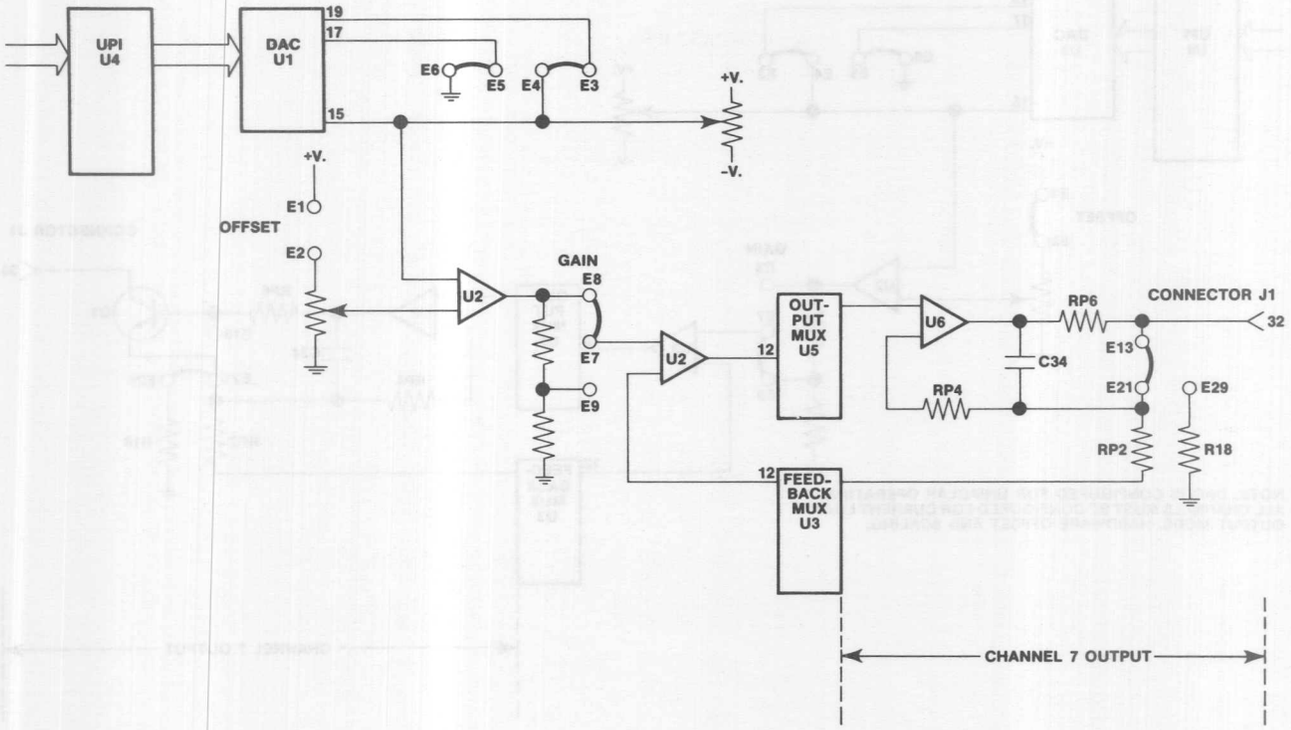


Figure 2-3. Jumper Configuration-Unipolar Voltage Output Mode

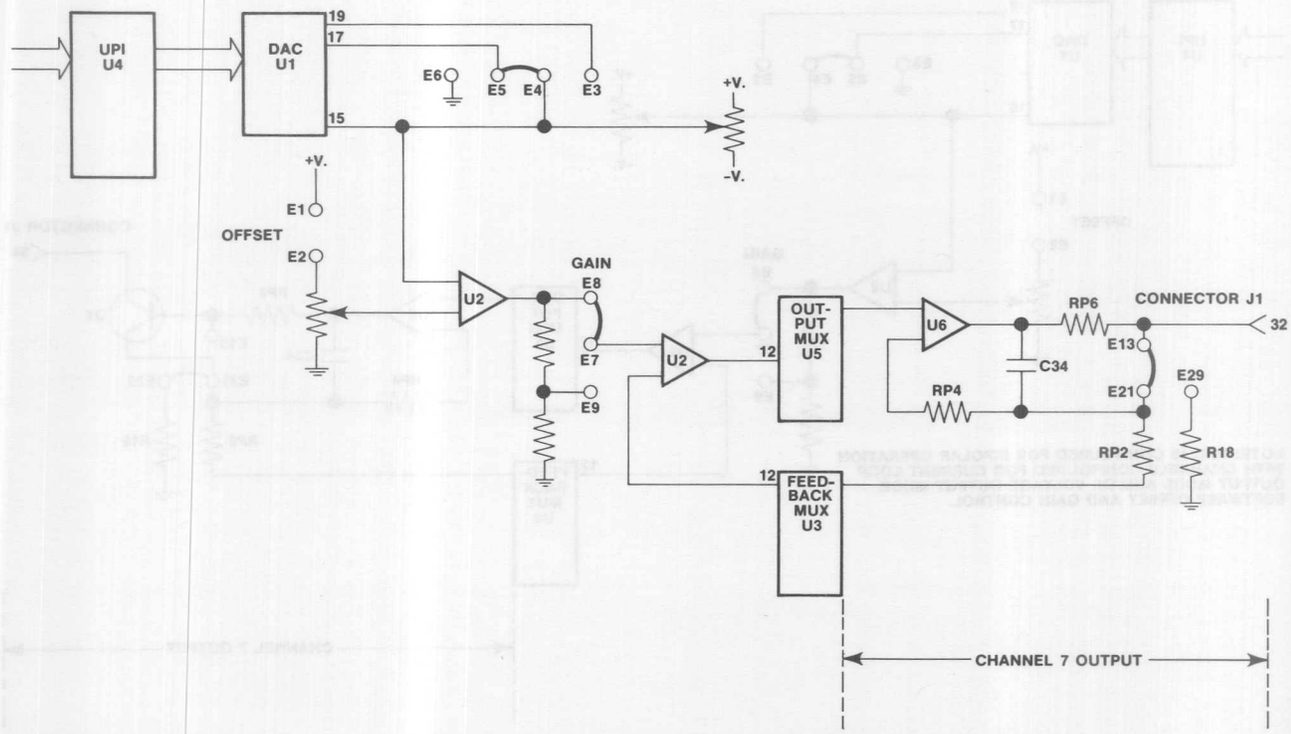


Figure 2-4. Jumper Configuration-Bipolar Voltage Output Mode

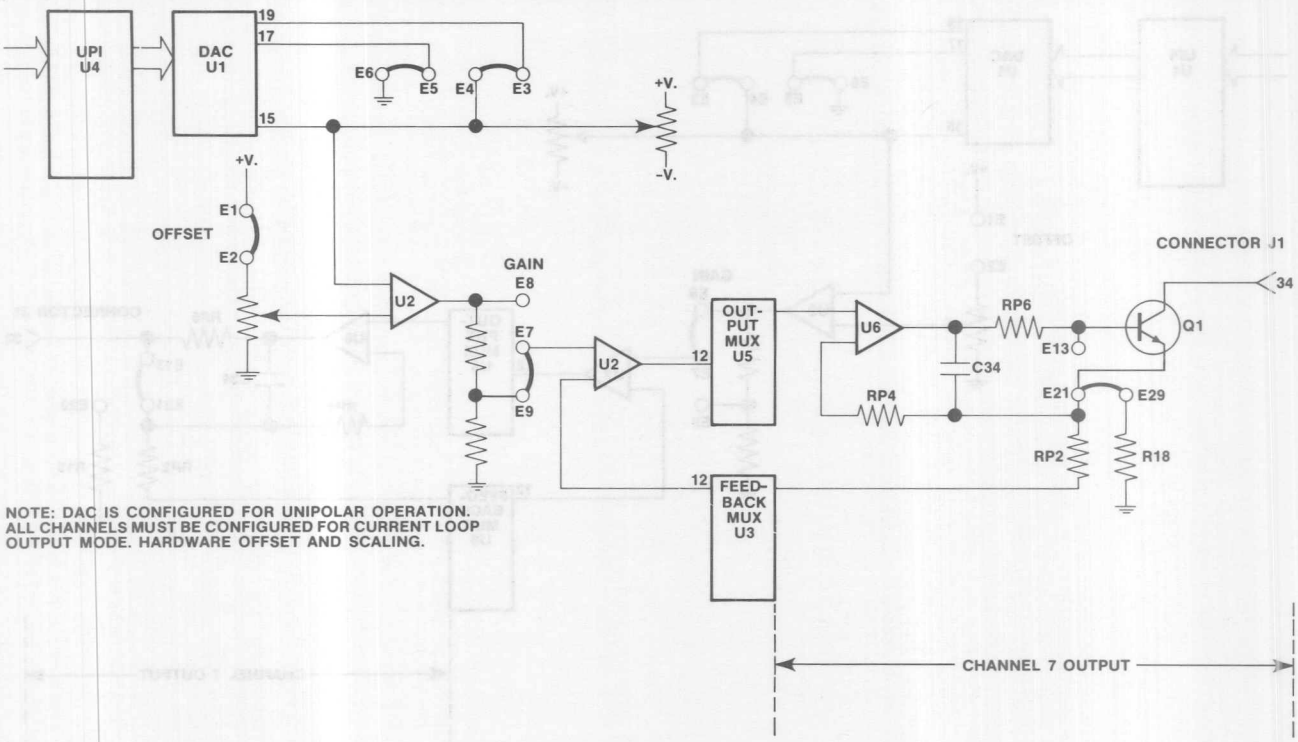


Figure 2-5. Jumper Configuration-Current Loop Output Mode, Hardware Offset/Gain

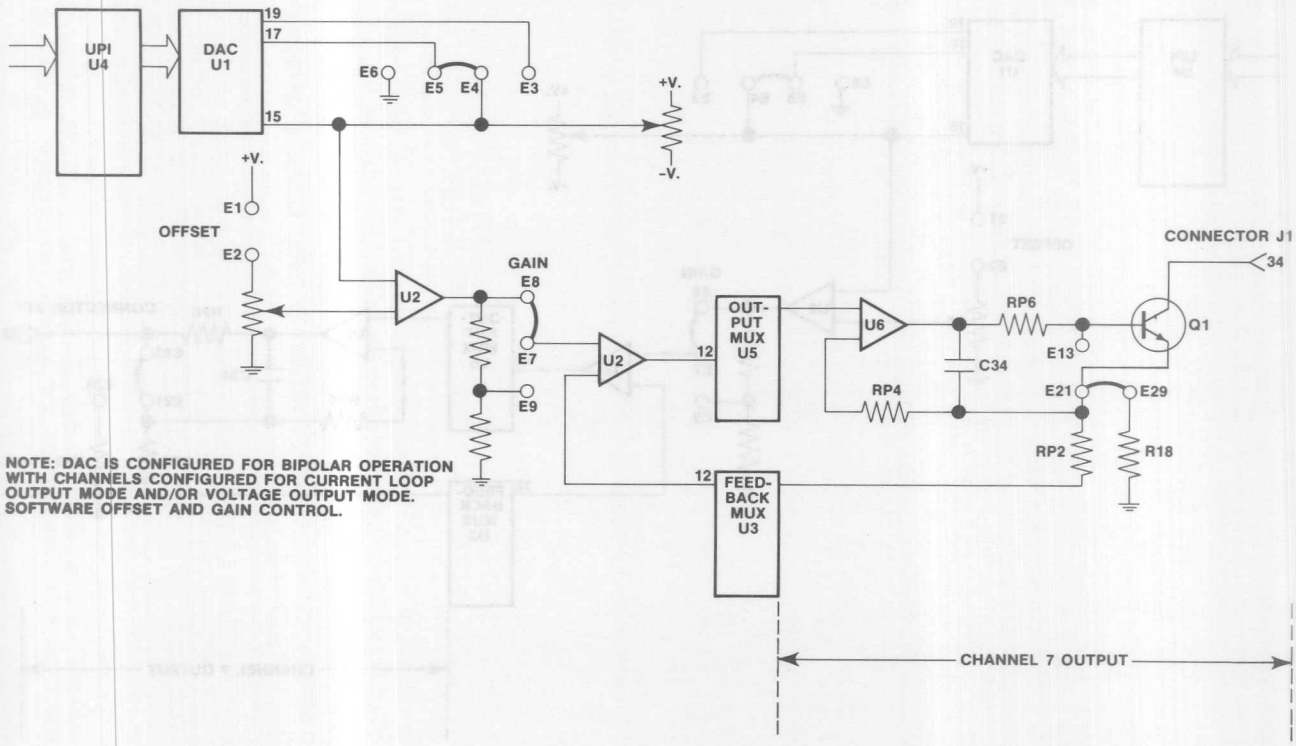


Figure 2-6. Jumper Configuration-Current Loop Output Mode, Bipolar, Software Offset/Gain

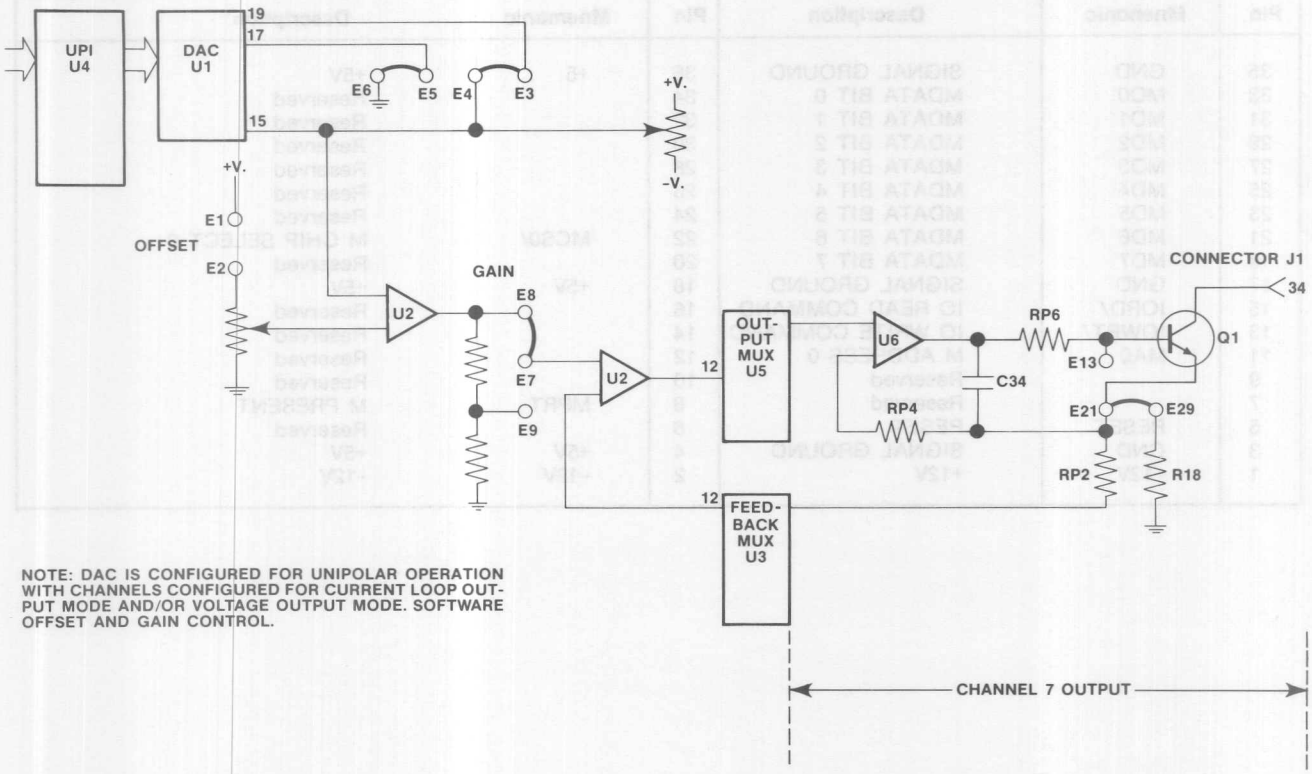


Figure 2-7. Jumper Configuration-Current Loop Output Mode, Unipolar, Software Offset/Gain

Channel Output Mode. The type of signal output from the buffer amplifiers (U6 and U7) is jumper selectable via three jumper posts at the output of each channel. These jumper posts allow the user to configure the output of each channel to either current loop output mode or voltage output mode. Table 2-2 lists the jumpers for each channel and their functions.

As an example, when E20 is jumpered to E28, channel 0 operates in the voltage output mode. In this mode, the buffer amplifier performs as a unity gain storage register for the DAC channel output voltage. When jumper posts E20 and E28 are disconnected and E28 and E36 are connected together, channel 0 operates in a current loop output mode. In this mode, the buffer amplifier functions as a 4 to 20 mA current converter, buffering the sample-and-hold capacitors and maintaining a constant voltage across the sampling resistors (R18 through R25).

2-10. CONNECTOR CONFIGURATION

The Multimodule board contains two connectors, the iSBX bus connector (P1) and the 50-pin edge connector (J1). Each of these is described in the following paragraphs.

The iSBX bus connector (P1) interfaces the Multimodule board to any host iSBC microcomputer that contains an iSBX bus connector. The signals found on each pin of connector P1 are listed in table 2-3 and described in Chapter 4.

Connector J1 interfaces the Multimodule board to the application via user-supplied data lines (channels). The channel output found on each pin of connector J1 is listed in table 2-4. Table 2-5 contains a listing of the details for compatible connectors that may be user-supplied to interface the J1 connector on the Multimodule board to an application.

Table 2-3. iSBX™ BUS Pin Assignment

Pin	Mnenonic	Description	Pin	Mnemonic	Description
35	GND	SIGNAL GROUND	36	+5	+5V
33	MD0	MDATA BIT 0	34		Reserved
31	MD1	MDATA BIT 1	32		Reserved
29	MD2	MDATA BIT 2	30		Reserved
27	MD3	MDATA BIT 3	28		Reserved
25	MD4	MDATA BIT 4	26		Reserved
23	MD5	MDATA BIT 5	24		Reserved
21	MD6	MDATA BIT 6	22	MCS0/	M CHIP SELECT 0
19	MD7	MDATA BIT 7	20		Reserved
17	GND	SIGNAL GROUND	18	+5V	+5V
15	IORD/	IO READ COMMAND	16		Reserved
13	IOWRT/	IO WRITE COMMAND	14		Reserved
11	MA0	M ADDRESS 0	12		Reserved
9		Reserved	10		Reserved
7		Reserved	8	MPRT	M PRESENT
5	RESET	RESET	6		Reserved
3	GND	SIGNAL GROUND	4	+5V	+5V
1	+12V	+12V	2	-12V	-12V

Table 2-4. Connector J1 Pin Assignment

Pin	Voltage Output Mode	Current Loop Output Mode	Pin	Voltage Output Mode	Current Loop Output Mode
1	Not Used	Not Used	2	Not Used	Not Used
3	Analog Return	Not Used	4	Channel 0 data	Not Used
5	Analog Return	Not Used	6	Not Used	Channel 0 data
7	Analog Return	Not Used	8	Channel 1 data	Not Used
9	Analog Return	Not Used	10	Not Used	Channel 1 data
11	Analog Return	Not Used	12	Channel 2 data	Not Used
13	Analog Return	Not Used	14	Not Used	Channel 2 data
15	Analog Return	Not Used	16	Channel 3 data	Not Used
17	Analog Return	Not Used	18	Not Used	Channel 3 data
19	Analog Return	Not Used	20	Channel 4 data	Not Used
21	Analog Return	Not Used	22	Not Used	Channel 4 data
23	Analog Return	Not Used	24	Channel 5 data	Not Used
25	Analog Return	Not Used	26	Not Used	Channel 5 data
27	Analog Return	Not Used	28	Channel 6 data	Not Used
29	Analog Return	Not Used	30	Not Used	Channel 6 data
31	Analog Return	Not Used	32	Channel 7 data	Not Used
33	Analog Return	Not Used	34	Not Used	Channel 7 data
35	Not Used	Not Used	36	Not Used	Not Used
37	Not Used	Not Used	38	Not Used	Not Used
39	Not Used	Not Used	40	Not Used	Not Used
41	Not Used	Not Used	42	Not Used	Not Used
43	Not Used	Not Used	44	Not Used	Not Used
45	Not Used	Not Used	46	Not Used	Not Used
47	Not Used	Ext. Supply Return	48	Not Used	Ext. Supply Return
49	-12V	-12V	50	+12V	+12V

Note: All odd-numbered pins (1,3,...49) are on component side of the board. Pin 1 is the right-most pin when viewed from the component side with the board extractors at the top.

Table 2-5. Compatible J1 Connector Details

Function	No. of Pairs Pins	Centers (Inches)	Connector Type	Vendor	Vendor Part No.
Parallel I/O Connector	25/50	0.1	Female Flat Crimp	3M AMP ANSLEY SAE	3415-0001 W/O EARS 88083-1 609-5015 SD6750 SERIES
Parallel I/O Connector	25/50	0.1	Female Soldered	AMP VIKING TI	2-583485-6 3KH25/9JN5 H312125
Parallel I/O Connector	25/50	0.1	Female Wirewrap	TI VIKING ITT CANNON	H421011-25 3KH25/JND5 EC4A050A1A

2-11. BOARD INSTALLATION

The Multimodule board mounts directly onto a host iSBC microcomputer by means of an iSBX bus connector. Figure 2-8 shows the assembly of the mounting screws and spacer. Install the board onto a host iSBC microcomputer as follows:

CAUTION

Remove power from the system before inserting or removing iSBC microcomputer boards into/from a cardcage. Failure to do so could result in damage to the boards.

a. With a plastic screw, 1/4 by 6-32, secure the plastic 1/2 by 6-32 spacer to the host iSBC board.

b. Locate pin 1 of the iSBX bus connector (P1) on the Multimodule board and align it with pin 1 of the iSBX bus connector on the host iSBC microcomputer.

c. Align the mounting hole on the Multimodule board with the mounting spacer installed onto the host iSBC board in the first step.

d. Gently press the two boards together until the connector seats.

e. Secure the Multimodule board to the top of the spacer with another plastic 1/4 by 6-32 screw.

NOTE

The location of an installed Multimodule board and the iSBX bus connector number on the host iSBC microcomputer may vary according to the type of host iSBC microcomputer that is used.

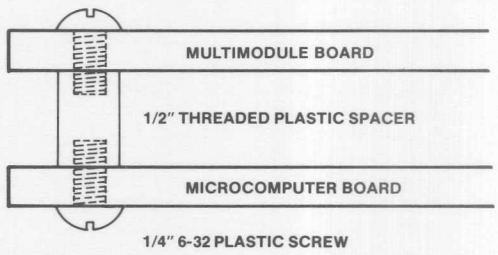


Figure 2-8. Mounting Technique

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

This chapter describes the programming of the iSBX 328 Analog Output Multimodule Board. Included are sections on addressing, programming requirements, interrupt servicing, and programming examples. More information on programming of the 8401 UPI device is contained in the Intel *UPI-41 User's Manual, Order No. 9800504.* Appendix A at the end of this text contains a sample program for use in calibrating the iSBX 328 board.

3-2. ADDRESSING

The host iSBC microcomputer addresses the Multimodule board by executing an IN or OUT instruction specifying one of the legal port addresses. Table 3-1 lists all of the legal port addresses for the Multimodule board. Since some host iSBC microcomputers will accept more than one Multimodule board, the upper address byte for each iSBX bus connector must vary, as table 3-1 shows.

3-3. PROGRAMMING SEQUENCE

The programming sequence required by the board is relatively straight-forward. In order to output converted data onto one of the channels, the user first must configure the Multimodule board jumpers to allow operation suitable for the application and then perform the following operations in the sequence listed. Each operation is detailed further in subsequent paragraphs of the text.

1. Check the status from the Multimodule board to ensure that the board is ready to accept an initialization byte from the host iSBC microcomputer board. Status bit 3 (F0) is HIGH when the UPI is ready to accept the initialization byte.
2. Initialize the UPI device for proper operation during the data output sequence. This includes selecting the number of channels to be scanned and selecting one of the 3 resident programs within the UPI to be run.
3. Transfer the LOW BYTE of the data to the selected channel. This entails placing the digital data from the host iSBC microcomputr into the UPI device and allowing the firmware to decode and save it until the HIGH BYTE is received.
4. Check the status of the Multimodule board on completion of the operation. This consists of user programming that allows the host iSBC microcomputer board to read the status byte from the Multimodule board on completion of the data conversion and transfer sequence. The next byte of data cannot be transferred to the UPI device until the input buffer is not full (IBF=0).
5. Transfer the HIGH BYTE of data to the selected channel. This entails placing the digital data from the host iSBC microcomputer into the UPI device and allowing the firmware to combine it with the LOW BYTE (previously converted) and send it to the proper channel address.
6. Check the status of the Multimodule board on completion of the operation. This consists of reading the status byte from the Multimodule board on completion of the data conversion and transfer sequence and checking for IBF=0.

Table 3-1. I/O Port Addresses

Function	8-Bit Port Address	16-Bit Port Address	Comments
READ STATUS	X1,X3,X5, or X7	X2,X6,XA, or XE	READ contents of status register from UPI.
WRITE DATA	X0,X2,X4, or X6	X0,X4,X8, or XC	WRITE data, initialization word, low byte, or high byte to UPI.
WRITE RESET	X1,X3,X5, or X7	X2,X6,XA, or XE	WRITE any data pattern to the Multimodule board to reset UPI.

3-4. UPI INITIALIZATION SEQUENCE

To begin a data transfer operation, the user must, through programming, initialize the UPI device before the Multimodule board can begin accepting output data from the host iSBC microcomputer. The process of initializing the board for an output operation (after a power-on RESET or a software RESET) is performed by issuing an initialization byte to the UPI. The initialization byte for the UPI selects the firmware program that the UPI will perform (whether program 1, 2, 3, or 4) and the address of the last channel to be serviced (from 1 to 8). Figure 3-1 shows the format of the initialization byte required by the UPI and includes both the mode and last channel address fields.

MODE SELECT. Bits 3 and 4 of the initialization byte (refer to figure 3-1) select which type of configuration and offset generation is to be used during the operation by allowing one of four firmware programs within the UPI to be run. The UPI firmware uses bits 3 and 4 to determine what type of current offset generation it is working with and what mode of operation the channel is operating in (whether current loop output mode or voltage output mode).

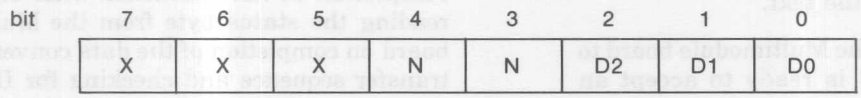
When bits 3 and 4 are LOW, program 1 is selected within the UPI firmware. This program assumes that the on-board DAC is configured to operate as unipolar and that the channel configurations are mixed; i.e., some channels are configured for operation in the voltage output mode and some in the current loop output mode. This routine does not attempt to alter the data destined for a voltage output channel, however, data for a current loop output channel is scaled and offset.

When bit 3 is HIGH and bit 4 is LOW, program 2 within the firmware is selected for operation. This program assumes that the board is configured for either unipolar or bipolar operation and that all channels are configured for operation in the voltage or hardware current loop output mode. This program within the firmware does not attempt to offset or scale the data output from the UPI.

When bit 3 is LOW and bit 4 is HIGH, program 3 within the firmware is selected for operation. This program assumes that the on-board DAC is configured to operate as bipolar and that the channel configurations are mixed; i.e., some channels are configured for operation in the voltage output mode and some for the current loop output mode. This program does not attempt to alter the data destined for a voltage output channel, however, data for a current loop output channel is scaled and offset.

When both bit 3 and bit 4 are HIGH, the utility test sequences within the firmware are initiated and allowed to perform one test cycle. The program allows the UPI to transfer input data directly out the output.

CHANNEL ADDRESS SELECT. Bits 0, 1, and 2 of the initialization byte provide the user with a means of selecting how many of the 8 channels are



NN: bit 3 4

=0 0 calls program 1 within the firmware that generates a software current offset for a unipolar configuration of the board in current loop output mode, or no offset generation in a unipolar configuration of the board in voltage output mode.

=0 1 calls program 2 within the firmware that generates hardware current offset if only the current loop output mode is used.

=1 0 calls program 3 within the firmware to generate a software current offset for a bipolar configuration of the board in current loop output mode, or no offset generation in voltage output mode.

=1 1 calls the test program within the firmware which operates the firmware utility test routines for the UPI.

D0-D2: gives a binary decode of last channel address to be scanned.

Figure 3-1. Initialization Byte Format

to be scanned. The firmware decodes bits 0, 1, and 2 as a binary count and scans a channel for each count, starting with channel 0. Any number of channels from one to eight may be selected and scanned, however, the channels selected to be scanned must be consecutive addresses starting from address 0. The channel scanning speed is inversely proportional to the number of channels selected; i.e., a four-times greater scanning speed can be attained with a one-channel scan than with a four-channel scan. In general, a faster scan rate can be attained by executing program 2 within the firmware; the UPI is not required to perform as many operations on the data. The remaining 3 bits of the initialization byte are unused and may be ignored.

3-5. DATA TRANSFER SEQUENCE

Data is transferred from the host iSBC microcomputer to the Multimodule board in a two byte format as depicted by the HIGH BYTE and the LOW BYTE in figure 3-2. Each output to the Multimodule board must include two bytes of data; the firmware within the UPI device on the Multimodule board requires that the LOW BYTE be received first so that the board can begin decoding the DAC channel address as early as possible. The functions performed by each of the data bytes is described in the following paragraphs.

When a HIGH BYTE is loaded into the input buffer in the UPI device, it contains the upper 8 bits (bits D11 through D4) of the 12-bit data word that is to be converted to an analog output.

The LOW BYTE includes the lower 4 bits (bits D3 through D0) of the data word, the 3-bit address of the DAC channel (bits A3, A2, and A1) to which the data is sent, and the mode indicator bit (M). The condition of the mode indicator bit (M) must comply with the mode of operation selected in the initialization byte (bits "NN"). The M bit, bit 0 of the LOW BYTE, selects the operating mode for that channel of the Multimodule board addressed by bits 1 through 3 of the LOW BYTE, as follows. When LOW, the M bit indicates to the firmware that the channel is to operate in the current loop output mode with the 8041 UPI generating the current offset and gain. When HIGH, the M bit indicates to the firmware that the channel is to operate in either the voltage output mode or the current loop output mode with current offset generated on the host iSBC microcomputer. If program 2 is selected (NN = 01), the state of bit 0 of the low byte does not matter; it is not checked by the UPI firmware.

3-6. STATUS CHECKING SEQUENCE

The Multimodule board includes a status word as shown in figure 3-3. The status word for the Multimodule board is read into the host iSBC microcomputer by issuing an IN command specifying one of the legal status port addresses for the Multimodule board.

Bit 1 of the status byte (IBF) indicates the condition of the input buffer within the UPI on the Multimodule board and should be checked before every data transfer from the host to the Multimodule board, including a check before initializaiton byte transfer. When data is transferred from the host iSBC microcomputer to the input buffer within the UPI device, the status of the input buffer is reported as "full"; i.e., bit 1 of the status byte is raised to indicate input buffer full (IBF=1). The IBF flag in the status byte is cleared by the UPI when it reads the data from the input buffer and begins processing it.

Bit 2 of the status byte (F0) is defined as the Ready-For-Initialization-Word indicator. When raised (F0=1), the bit indicates that the UPI is ready to accept the initialization word.

Bit 4 of the status byte (S0) is defined as the high-byte/low-byte indicator. When raised (S0=1), the bit indicates that the Multimodule board is requesting the HIGH (most significant) BYTE of the data to be present on the bidirectional data bus. Conversely, when LOW, S0 requests the LOW BYTE of data to be placed onto the data bus.

Bits 5 and 6 of the status byte (S1, S2) provide error indications for the utility test program within the firmware. When S1=1, an error is indicated on the checksum test that the firmware performs on the RAM internal to the UPI device; S1=0 indicates that the checksum test detected no problem within the RAM. When S2=1, an error is indicated on the RAM test performed by the firmware on the RAM internal to the UPI device; again, S2=0 indicates no error. The remaining three bits are unused and should be ignored when checking status.

Software on the host iSBC micrcomputer may use the IBF and S0 flags in the status word to provide a handshaking system when transferring data to the Multimodule board. The programming examples provided later in this chapter show methods of checking the status byte to determine the condition of the UPI device.

bit	7	6	5	4	3	2	1	0
LOW BYTE	D3	D2	D1	D0	A2	A1	A0	M

D3-D0: The lower 4 bits of the data to be transferred to the selected channel address.

A2-A0: DAC channel address to receive the converted data bits.

M: Not used if firmware is operating in program 2 (NN = 01).
= 0 for 8041 UPI generation of offset in current loop output mode.
= 1 for voltage output mode or host iSBC microcomputer generation of the offset in current loop output mode.

bit	7	6	5	4	3	2	1	0
HIGH BYTE	D11	D10	D9	D8	D7	D6	D5	D4

D11-D4: The upper 8 bits of the data to be transferred to the selected channel address.

Figure 3-2. Data Byte Formats

bit	7	6	5	4	3	2	1	0
	X	S2	S1	S0	X	F0	IBF	X

S1: 1 = error on ROM Checksum Test.
0 = no error on ROM Checksum Test

S2: 1 = error on RAM Test
0 = no error on RAM Test

S0: 1 = Multimodule board expects high byte.
0 = Multimodule board expects low byte.

F0: 1 = UPI ready for initialization word.
0 = UPI not ready for initialization word.

IBF: 1 = UPI input buffer full.
0 = UPI input buffer not full.

Figure 3-3. Status Word Format

3-7. INTERRUPTS

The Multimodule board contains no means of issuing a direct interrupt request to a host iSBC microcomputer. Data transfer coordination between the host and the Multimodule board must be performed via software polling of the status byte by the host. The IBF, S0, and F0 status bits from the UPI will give the required information to determine the status of the UPI device and the status of last operation that was issued to the Multimodule board. The S0 bit indicates which of the two bytes of data is required by the Multimodule board.

NOTE

It is important that the software operating within the host iSBC microcomputer check the IBF status bit before each byte of data is transferred to the Multimodule board. This will ensure that the input buffer within the UPI is available to accept the next byte of data.

3-8. PROGRAMMING EXAMPLES

The programming examples in the following paragraphs are listed in the form of subroutines, each of

which performs a programming function on the Multimodule board. Examples are included for issuing a RESET to the board, for issuing an initialization word to the UPI on the board, and for issuing data to the UPI on the board. Included within the routines are typical status checking methods that must be used to monitor the condition of the Multimodule board. The port addresses within the examples are listed with an "X" in the upper digit. Refer to the reference manual for the respective host iSBC microcomputer board to determine the value of "X" in the port address.

3-9. RESET PROGRAMMING EXAMPLE

The RESET command is issued to the Multimodule board by executing, on the host iSBC microcomcomputer, an OUT instruction that is directed to the status port address for the Multimodule board, as listed in table 3-1. When the RESET command is performed, it clears the READY flag (F0) in the status byte. Table 3-2 lists a typical RESET subroutine, however the port addresses may change depending on the iSBX connector and the type of host board used.

3-10. INITIALIZATION WORD PROGRAMMING EXAMPLE

Table 3-3 contains a typical subroutine for sending an initialization word to the UPI. Bear in mind that the port addresses shown in the example in table 3-3 may have to be changed for the application, depending on the type of host iSBC microcomputer used.

3-11. WRITE DATA PROGRAMMING EXAMPLE

Table 3-4 lists a typical subroutine for sending data to the UPI on the Multimodule board. The port addresses may have to be changed to fit the application, depending on the requirements of the host iSBC microcomputer.

Table 3-2. Typical RESET Subroutine

```
;This routine issues a RESET command to the Multimodule board.
;Uses-A, STATUS; Destroys-Nothing.
        PUBLIC    RESET
        STATUS    EQU     X1H     ;Defines status port address
RESET:  OUT       STATUS          ;Write to the UPI status port,
                                  ;contents of A register is not
                                  ;important
        RET
```

Table 3-3. Typical Initialization Word Routine

```
;INIT outputs an initialization word from A to the 8041 UPI port upon
;recognition of the READY flag.
;Uses-A, STATUS, RYMASK; Destroys-Nothing.
        PUBLIC    INIT
        STATUS    EQU     X1H     ;Defines status port address
        RDMASK    EQU     4       ;Defines READY flag mask
        DATAD     EQU     X0H     ;Definies Data port address
INIT:   IN        STATUS          ;Read UPI status byte
        ANI       RYMASK          ;Check for UPI READY status
        JZ        INIT            ;Waiting for READY status
        MVI       A,OFH           ;Load initialization word into A,
                                  ;set UPI to Voltage-only mode and 8
                                  ;channel scan
        OUT       DATAD           ;Send initialization word to data
                                  ;port
        RET
```

Table 3-4. Typical Data Output Subroutine

```
;ODATA outputs data from A to the UPI on the Multimodule board.
;Uses-A, STATUS, IBMASK, BASAD; Destroys-Nothing.

        PUBLIC    ODATA

STATUS  EQU       X1H     ;Defines status port address
BASAD   EQU       X0H     ;Defines data port address
IBMASK  EQU       2       ;Defines Input-Buffer-Full flag mask

ODATA:  IN        STATUS  ;Read UPI status byte
        ANI       IBMASK  ;Mask for IBF bit of status
        JNZ       ODATA   ;Wait for IBF not full
        MOV       A,B     ;Load data byte from B register
                          ;into A
        OUT       BASAD   ;Send the data in A to the UPI
        RET
```

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a functional description of the interface signals and a detailed circuit analysis for the iSBX 328 Analog Output Multimodule Board. The functional description of the board includes details on the operation of each of the major components on the board. Figure 4-1 shows a functional block diagram of the interaction between the major components of the Multimodule board.

4-2. iSBX™ BUS INTERFACE SIGNAL DESCRIPTION

Programmed control of the iSBX 328 Analog Output Multimodule Board is achieved by controlling the signals that interface to and from the Multimodule board via the iSBX bus connector. The iSBX bus signals that interact with the Multimodule board and their functions are detailed in the following paragraphs.

RESET (Reset) — This active high signal, when asserted to the Multimodule board, resets the 8041 UPI device on the board. Since the UPI device operates from a free-running clock, it will immediately begin program execution when the RESET signal is removed. Notice that the RESET signal is inverted by Q9, R15, and R16 on the Multimodule board to create a negative-true RESET signal, as required by the UPI device.

MD0-MD7 (Bidirectional Data Bus) — These eight bidirectional data lines provide a means of transferring commands, status, and data between the UPI device on the Multimodule board and the host iSBC microcomputer.

IORD/ (Read Command) — This active low signal is generated by the host iSBC microcomputer as a command to the Multimodule board to input data via the bidirectional data bus (MD0-MD7) to the host. The IORD/ signal enables the UPI device to input data from the bidirectional data bus into an internal Input Buffer Register or to output data from an internal Status register onto the bidirectional data bus.

IOWRT/ (Write Command) — This active low signal is generated by the host iSBC microcomputer as a command to the Multimodule to accept data present on the bidirectional data bus. The IOWRT/ signal causes the UPI device to accept data into its Data Bus Buffer register from the bidirectional data bus.

MCS0/ (Select) — MCS0/ is an active low input signal to the Multimodule board to enable the board to accept either an IORD/ or IOWRT/ command from the host iSBC microcomputer board.

MA0 (Funtion Selector) — This active high input from the host iSBC microcomputer, in conjunction with the IORD/ and IOWRT/ signals, selects whether the data byte on the bidirectional bus is to be treated as data or command input.

4-3. FUNCTIONAL DESCRIPTION

The functional description is based upon the functional block diagram shown in figure 4-1. Each functional block in the figure is explained in detail in the following paragraphs.

4-4. 8041 UNIVERSAL PERIPHERAL INTERFACE

The 8041 UPI device (U4) is a single-chip microcomputer that contains 1024 bytes of program memory, 64 bytes of data memory, 18 I/O lines, an 8-bit CPU, an event timer, and a clock oscillator within a single 40-pin LSI package. The UPI is driven with the dedicated on-board clock (Y1) at a rate of 6 MHz. The firmware supplied with the UPI enables it to operate as a controller in accepting commands from the host iSBC microcomputer and performing data transfers to the analog application. Data from the host iSBC microcomputer board is translated within the UPI into a 12-bit DAC word and a 4-bit multiplexer control word from port 1 and port 2 of the UPI device. The data transfer handshaking is performed via the Input Buffer Full (IBF) and the High/Low-Byte (S0) indicators within the status byte. More information on the programming of the UPI device is contained in Chapter 3 of this text.

4-5. DIGITAL-TO-ANALOG CONVERTER

The DAC (U1) converts 12 bits of digital input code to a proportional current output from pin 15. The DAC data input lines are active LOW and cause a digital hexadecimal data input of FFFH to generate a zero current flow output from pin 15 of the DAC. By the same means, the DAC converts an input of 000 into a full scale current flow output. The magnitude of the full scale current flow is influenced by the reference voltage on pin 16, but will generally

range about -2 mA (the "minus" signifies that the DAC is operating as a current sink). The DAC contains internal resistors that perform current-to-voltage translations and that perform bipolar current offsetting funtions.

4-6. CURRENT-TO-VOLTAGE AMPLIFIER

The current-to-voltage translation is completed by amplifier U2 (pins 1, 2, and 3) and by two resistors internal to the DAC.

4-7. LOOP AMPLIFIER

The loop amplifier, U2 pins 5, 6, and 7, is used to provide feedback for the data output operation when the board is operating in either the voltage output or the current loop output mode. The feedback loop corrects for offsets and temperature effects induced by the various on-board devices in the path of the output signal.

4-8. FREQUENCY COMPENSATOR

The frequency compensation logic consists of capacitors C2, C3, and C9 and resistors R8 and R9. Together these devices form a feedback control network that allows a dc gain of approximately 20. The network controls the frequency response of the output to ensure a stable gain despite small variances in the sample-and-hold capacitance, the multiplexer resistance, and the load capacitance.

4-9. OUTPUT MULTIPLEXER

The output multiplexer (U5) gates the analog output data from U2 to one of eight channels, as selected by the UPI device. The multiplexer acts as a low resistance switch in providing an analog data signal to the sample-and-hold capacitors. Each channel is selected with a binary decode of the three least significant bits (bits 1, 2, and 3) of the port 2 output from the UPI device. The bit 0 output from the UPI (port 2) is used to enable the output multiplexer for operation.

4-10. BUFFER AMPLIFIERS

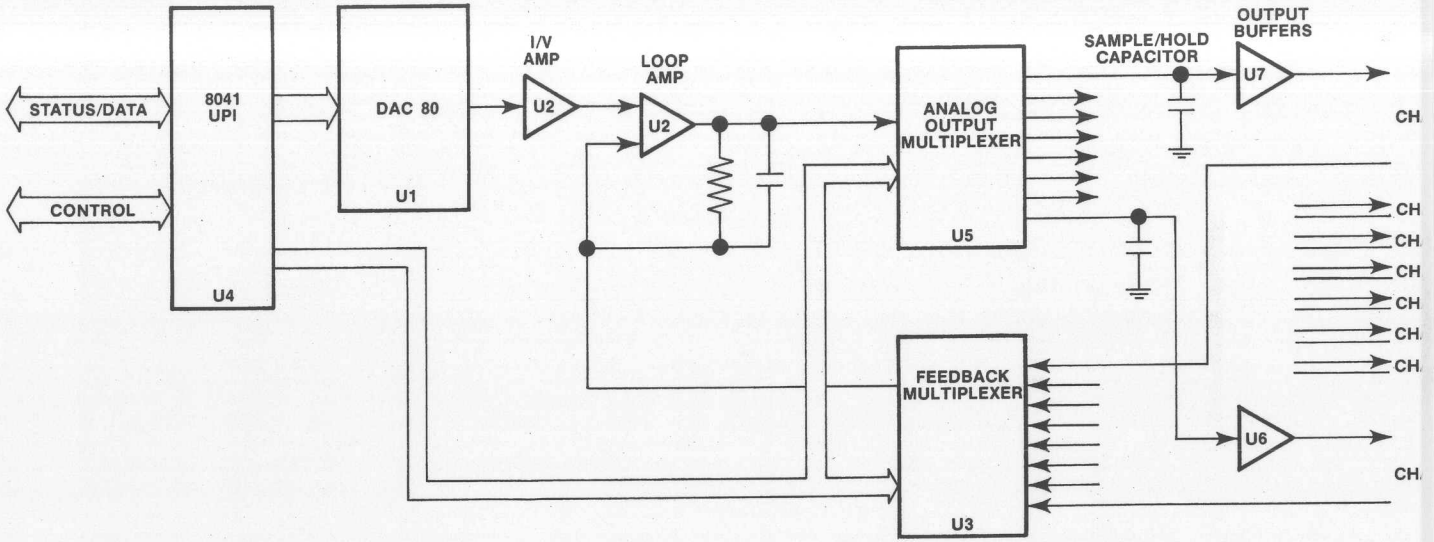
The buffer amplifiers (U6 and U7) are designed to supply a high impedance when providing data to the sample-and-hold capacitors to prevent a quick voltage decay when the channel is not selected. Depending on the jumper configuration, the buffers can operate as a unity-gain buffer amplifier in voltage output mode or as a 4 to 20 mA current converter, maintaining a constant voltage drop across the current-sampling resistors (R18 through R25). The two resistors and capacitor on each channel provide isolation from capacitive loads.

4-11. FEEDBACK MULTIPLEXER

The feedback multiplexer (U3) selects an output channel synchronous with the channel selection performed by the output multiplexer (U5); that is, when one channel is selected to receive output, it is also selected to provide feedback. Feedback from a channel enters the multiplexer on one of the eight inputs. If selected, the input is gated through the multiplexer and out pin 12. The feedback current then returns to the loop amplifier (U2) to provide loop error correction.

4-12. VOLTAGE-TO-CURRENT CONVERTER

The voltage-to-current converter consists of transistors Q1 thrugh Q8 and resistors R18 through R25. These components work together to convert the multiplexer voltage into a related current of 4 to 20 mA. A compliance voltage of 12 to 40 volts is acceptable, but current loop loads must be provided for voltages greater than 12 volts.



iSBX™ 328 Board Functional Block

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides a list of replaceable parts, service diagrams, adjustments, and service and repair assistance instructions for the iSBX 328 Analog Output Multimodule Board.

5-2. SERVICE AND REPAIR ASSISTANCE

United States Customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Offices or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other MCSD products, it is usually stamped on a label.

c. Serial number of product. On boards, this number is usually stamped on the board. On other MCSD products, the serial number is usually stamped on a label.

d. Shipping and billing addresses.

e. Purchase order number for billing purposes if your warranty has expired.

f. Information on extended warranty agreements, if applicable.

Use the following telephone numbers for contacting the Intel Product Service Hotline:

All U.S. locations, except Alaska, Arizona & Hawaii: (800) 528-0595

All other locations: (602) 869-4600

TWX Number: (910) 951-1330

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

5-3. ADJUSTMENT PROCEDURES

The adjustments for the iSBX 328 Analog Output Multimodule Board include facilities to allow the user to perform 3 adjustments; current loop offset, DAC offset, and voltage gain. The calibration procedure for each adjustment differs slightly, depending on whether the Multimodule board is configured for a voltage output mode application or a current loop output mode application. The procedures for each adjustment are outlined in the following paragraphs and assume that there is an offset adjustment subroutine (DACOFF) and a range adjustment subroutine (DACRNG), similar to those listed in Appendix A, resident within the program being executed on a microcomputer development system. Each Multimodule board is adjusted at the factory, however, the boards should be readjusted whenever reconfiguration occurs. The calibration procedure is preceded by a list of test equipment required to perform the calibration.

NOTE

When performing the adjustments for a board containing a mixed configuraiton (both voltage output channels and current loop channels) or for a board containing only voltage output channels, follow the adjustment procedure as described for the voltage output mode. Adjust the board as described for the current loop output mode only when *all* channels on the board are configured to operate as current loop channels.

5-4. TEST EQUIPMENT REQUIRED

The only test equipment required to adjust the gain and offset for the Multimodule board is a Digital Voltmeter (DVM) with a voltage range of 0 to 10

volts and an accuracy of ±0.005% or better. The procedure listed here also requires the use of an Intel microcomputer development system to provide an operating system for running the calibration programs and to provide power for the Multimodule board and the host iSBC microcomputer.

5-5. PRELIMINARY ADJUSTMENT PROCEDURE

The first step of the calibration procedure is to check the voltage levels for the dc supply voltages. The dc supply voltages are listed in table 5-1 and may be verified on the Multimodule board at the capacitors listed. If any of the power sources are out of tolerance, they should be readjusted before the calibration procedure is performed.

Table 5-1. Power Supply Voltage Checkpoints

Supply	Tolerance	Voltmeter Connection on Multimodule Board
+12V	±5%	Across C28
-12V	±5%	Across C27
+5V	±5%	Across C26
NOTE: Refer to figure 5-1 to locate capacitors		

5-6. VOLTAGE OUTPUT MODE OFFSET ADJUSTMENT

Connect the positive lead of the DVM to connector J1 pin-4 and the negative lead to connector J1 pin-3. CALL the offset adn adjustment subroutine (DACOFF in Appendix A) and adjust variable resistor R1 for either 0.0000 volts (unipolar operation) or -5.0000 volts (bipolar operation).

5-7. VOLTAGE OUTPUT MODE RANGE ADJUSTMENT

Connect the DVM as for the offset adjustment (positive to connector J1 pin-4, negative to J1 pin-3) and CALL the offset and adjustment subroutine (DACRNG in Appendix A) and adjust variable resistor R1 for either 4.9976 volts (unipolar operation) or -4.9988 volts (bipolar operation).

5-8. CURRENT LOOP OUTPUT MODE GAIN ADJUSTMENT

Connect positive lead of the DVM to the E36 and the negative lead to connector J1 pin-3. CALL the offset adjustment subroutine (DACOFF in Appendix A) and adjust variable resistor R3 to attain a reading of 0.6250 volts. If R3 does not carry the adjustment to 0.6250 volts, use resistor R1 to complete the adjustment.

5-9. CURRENT LOOP MODE OUTPUT RANGE ADJUSTMENT

Connect the DVM as for the offset adjustment (positive lead to the E36 and negative lead to connector J1 pin-3), and CALL the range adjustment subroutine (DACRNG in Appendix A). Adjust variable resistor R2 until a reading of 3.1244 volts is attained.

5-10. REPLACEABLE PARTS

Table 5-3 provides a list of replaceable parts for the Multimodule board. Table 5-2 identifies and locates the manufacturers specified in the MFR CODE column of table 5-3. Intel parts that are available on the open market are listed in the MFR CODE column as "COML". Every effort should be made to procure these parts from a local (commercial) distributor.

5-11. SERVICE DIAGRAMS

The parts location diagram and schematic diagrams for the Multimodule board are provided in figures 5-1 and 5-2, respectively. On the schematic diagram, a signal mnemonic that ends with a slash (e.g., MSCO/) is active LOW. Conversely, a signal mnemonic without the slash (e.g., OPTO) is active HIGH.

Table 5-2. Manufacturer Codes

Mfr. Code	Manufacturer	Address
AD	Analog Devices	Santa Clara, CA
BEC	Beckman Instruments	Cedar Grove, NJ
CCC	Crystek Crystal Corp.	Ft. Myers, FL
EMC	EMC Technology, Inc.	Cherry Hill, NJ
HAR	Harris Semiconductor	Dallas, TX
INTEL	Intel Corp.	Santa Clara, CA
MOT	Motorola	Phoenix, AZ
NAT	National Semiconductor	Santa Clara, CA
VIK	Viking Connector, Inc.	Chatsworth, CA
OBD	Order by description, any commercial (COML) source	

Table 5-3. Replaceable Parts

Reference Designator	Description	Mfr Part No.	Mfr Code	Qty
U4	IC, Universal Peripheral Interface	8041A	INTEL	11
U6, U7	IC, Quad BI FET Linear Op Amp	LF-347BN	NAT	2
U2	IC, Quad Linear Op Amp	LF-353BN	NAT	1
U3, U5	IC, Analog Multiplexer	HI-1818A	HAR	2
U1	IC, Digital-to-Analog Converter	DAC-80Z	AD	1
VR1	Diode, Zener 1N4576	1N4576	MOT	1
Q9	Transistor, PNP, 2N4403	OBD	COML	1
Q1-Q8	Transistor, NPN, Darlington, 2N6427	OBD	COML	8
Y1	Crystal, 6 MHz	CY6B	CCC	1
P1	Connector, 36-pin	68-357	VIK	1
	Socket, 20-pin, SIP	7195-295-5	EMC	2
	Socket, 12-pin, SIP	7195-295-5	EMC	2
	Socket, 8-pin, SIP	7195-295-5	EMC	2
	Socket, 7-pin, SIP	7195-295-5	EMC	4
E1-E37	Wirewrap stake pin	87022-1	AMP	37
	Shorting plugs	530153-2	AMP	12
RP1, RP2	Resistor pack, 1K, 8-pin, SIP ±2%	764-3-R1K	BEC	2
RP3, RP4	Resistor pack, 4.7K, 8-pin, SIP, ±2%	764-3-R4.7K	BEC	2
RP5, RP6	Resistor pack, 33 ohm, 8-pin, SIP, ±2%	764-3-R33	BEC	2
R1, R2	Resistor, adjustable, 20K	OBD	COML	2
R3	Resistor, adjustable, 200 ohm	OBD	COML	1
R4	Resistor, 1.6K, 0.1%, 1/20 W	OBD	COML	1
R5	Resistor, 464K, 1%, 1/8 W	OBD	COML	1
R7, R17	Resistor, 1.1K, 5%, 1/4 W	OBD	COML	1
R8	Resistor, 20K, 5%, 1/4 W	OBD	COML	1
R6, R12	Resistor, 196K, 1%, 1/8 W	OBD	COML	1
R9	Resistor, 3.6K, 5%, 1/4 W	OBD	COMI	1
R15, R16	Resistor, 10K, 5%, 1/4 W	OBD	COML	2
R10, R13, R14	Resistor, 10K, 0.1%, 1/20 W	OBD	COML	3
R11	Resistor, 39.2K, 1%, 1/8 W	OBD	COML	2
R18-R25	Resistor, 156.25 ohm, 0.02%, 1/20 W	OBD	COML	8
C1	Capacitor, 0.1 μF, +80 -20%, 50V, ceramic	OBD	COML	1
C2	Capacitor, 68 pF, 10%, 50V, ceramic	OBD	COML	1
C3, C8	Capacitor, 390 pF, ±10%, 50V, ceramic	OBD	COML	2
C5	Capacitor, 0.01 μF, +80 -20%, 50V, ceramic	OBD	COML	1
C9	Capacitor, 220 pF, ±10%, 50V, ceramic	OBD	COML	1
C11, C12	Capacitor, 22 pF, ±10%, 50V, ceramic	OBD	COML	2
C4, C6, C7, C13-C15	Capacitor, 1μF, +80 -20%, 50V, ceramic	OBD	COML	6
C10, C22-C24, C30-C33	Capacitor, 0.1 μF, +80 -20%, 50V, ceramic	OBD	COML	8
C16-C21, C25, C29	Capacitor, 0.22 μF, ±10%, 50V, ceramic	OBD	COML	8
C27, C28	Capacitor, 15 μF, ±20%, 20V, tant.	OBD	COML	2
C26	Capacitor, 33 μF, ±20%, 10V, tant.	OBD	COML	1
C34-C41	Capacitor, 470 pF, ±10%, 50V, ceramic	OBD	COML	8

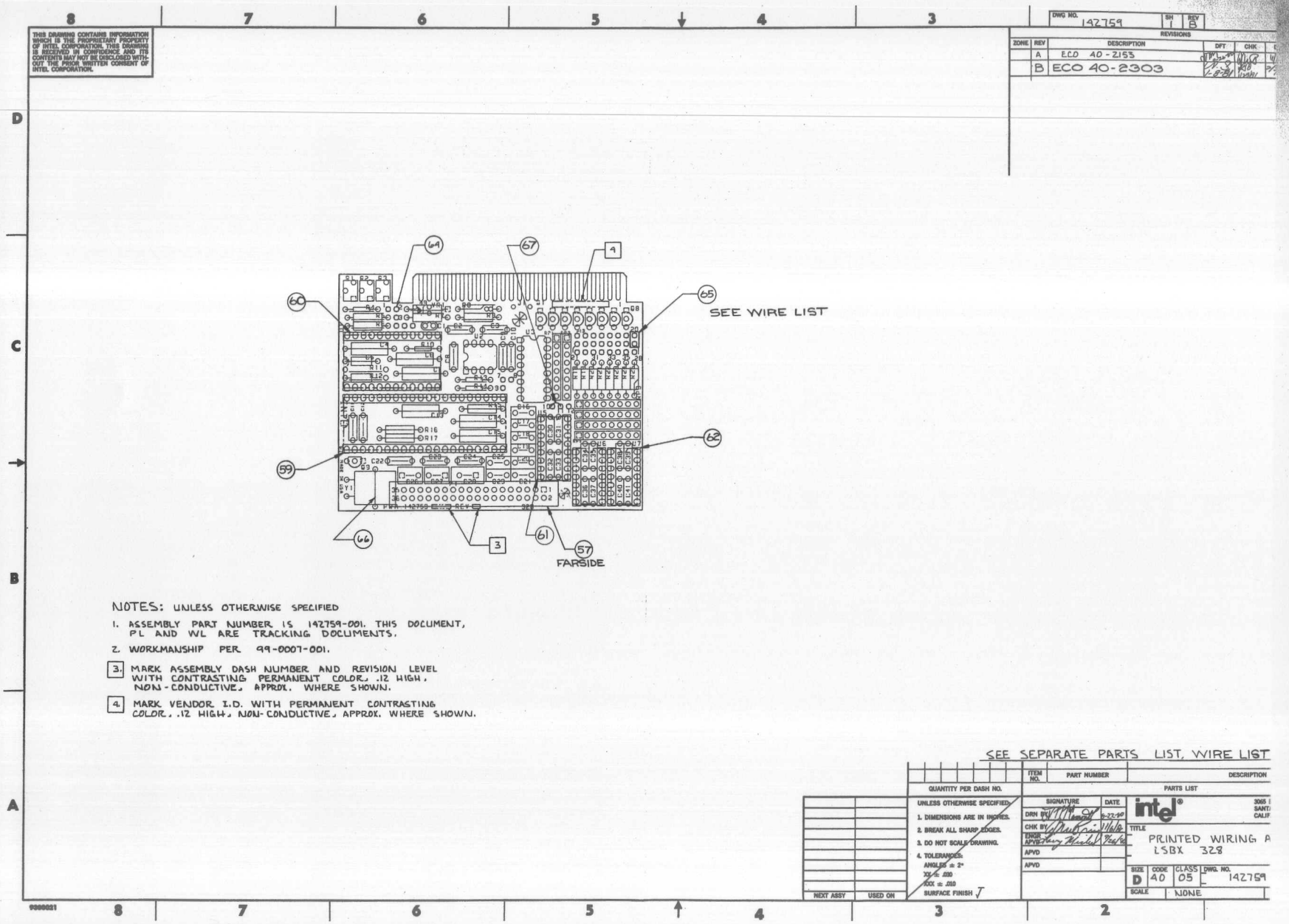


Figure 5-1. iSBX™ 328 Analog Output Multimodule™ Board Parts Locat

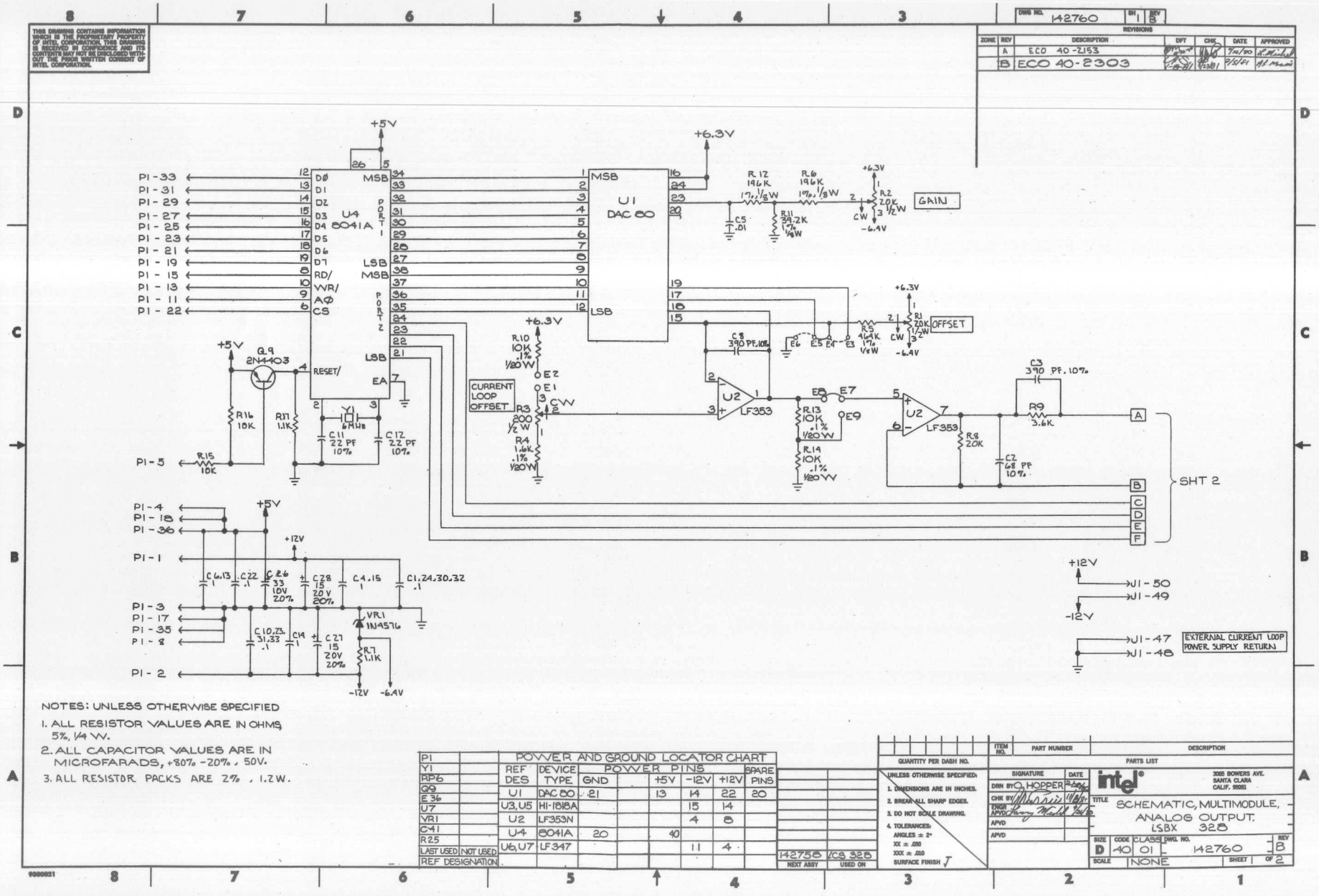


Figure 5-2. iSBX™ 328 Analog Output Multimodule™ Board Schematic Diagram (Sheet 1 of 2)

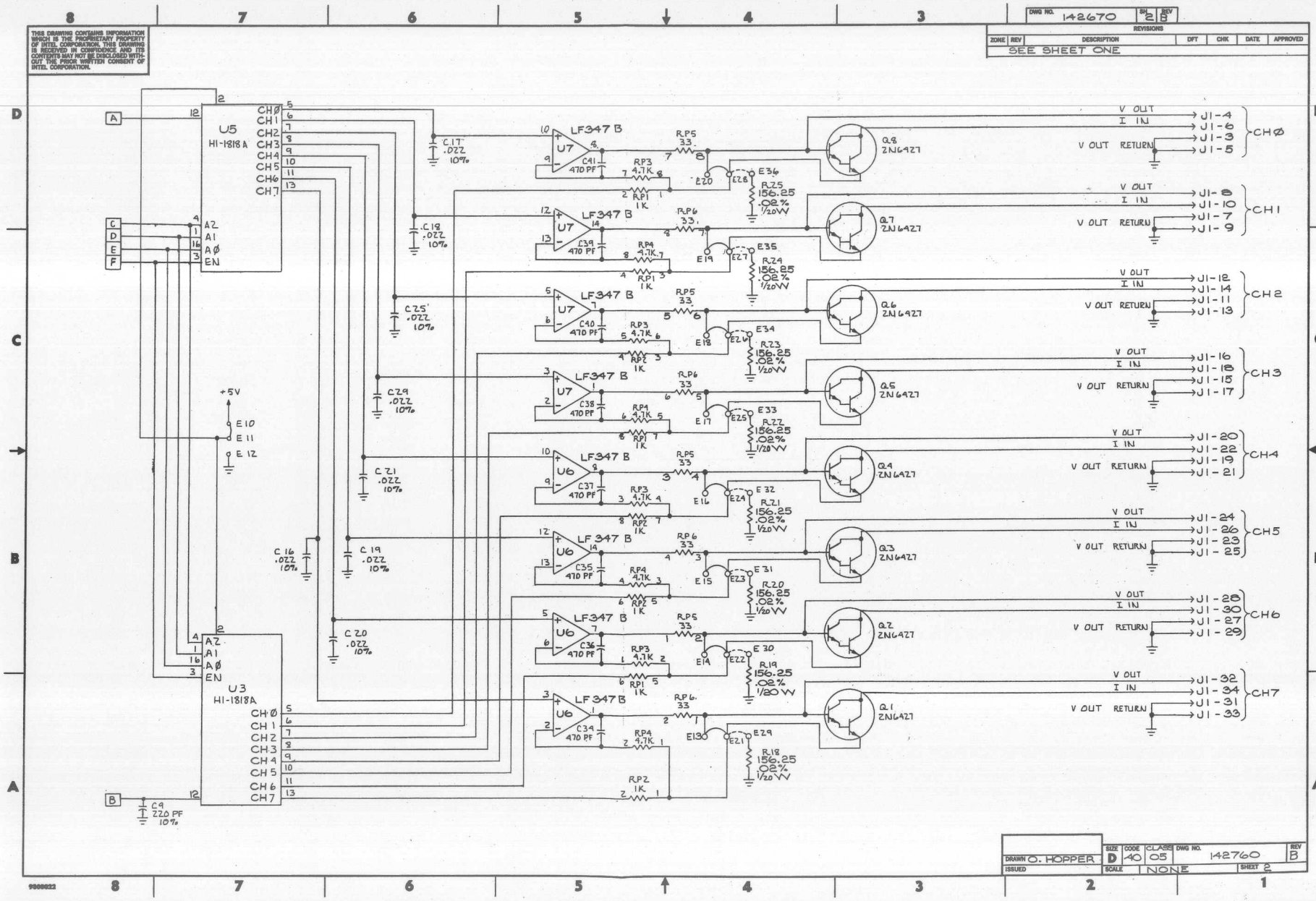


Figure 5-2. iSBX™ 328 Analog Output Multimodule™ Board Schematic Diagram (Sheet 2 of 2)

APPENDIX A

The programs listed in the following text are designed for use in an Intel microcomputer development system to allow calibration of the iSBX 328 Analog Output Multimodule Board. Table A-1 contains a range calibration program and table A-2 contains an offset calibration program. Calibration instructions are listed in Chapter 5 of the text.

Table A-1. RANGE Adjustment

This table contains subroutines for use in performing the RANGE adjustment for the iSBX 328 Analog Output Multimodule Board when installed into the J6 Multimodule Connector (closest to the center) of a host iSBC 80/24 board. To configure for another Multimodule Connector or host, modify the port addresses as specified in the hardware reference manual for the respective iSBC microcomputer board.

The DACRNG routine selects channel 0 and initializes it for operation. Data to be output on the channels is placed into the B register. The OUTRDY routine checks the status of the UPI and outputs the data contained in the B register successively to each channel selected. While the program is operating, the RANGE for the DAC may be adjusted as detailed in Chapter 5 of the text.

```
        PUBLIC      OUTRDY,     DACRNG
        STATUS      EQU         0F1H        ;Status Port Address
        DATA        EQU         0F0H        ;Data Port Address
        IBMASK      EQU         02H         ;IBF Mask

        CSEG
DACRNG: OUT         STATUS                  ;Software Reset
        MVI         B, 0BH                  ;Select number of channels to be scanned.
        CALL        OUTRDY                  ;Output when UPI ready

        MVI         B,0F0H                  ;Select channel 0, LOW BYTE = F0H
        CALL        OUTRDY                  ;Output when UPI Ready
        MVI         B,0FFH                  Select HIGH BYTE = FFH
        CALL        OUTRDY                  ;Output when UPI ready
        RET

OUTRDY: IN          STATUS                  ;Read status byte
        ANI         IBMASK                  ;Check for IBF = 1
        JNZ         OUTRDY                  ;Yes, check again
        MOV         A, B                    ;No, get data
        OUT         DATA                    ;Send data
        RET
```

Table A-2. OFFSET Adjustment

This table contains subroutines for use in performing the DAC OFFSET Adjustment for the iSBX 328 Analog Output Multimodule Board when installed into the J6 Multimodule Connector on a host iSBC 80/24 board. To configure for another Multimodule Connector or another host, modify the port addresses as specified in the hardware reference manual for the respective iSBC microcomputer board.

The DACOFF routine selects channels 0 for operation. Data to be output on the channels is placed into the B register. The OUTRDY routine then checks the status of the UPI and outputs the data. While the program is operating, the OFFSET for the DAC may be adjusted as detailed in Chapter 5 of the text.

```
                PUBLIC      OUTRDY,     DACOFF
                STATUS      EQU         0F1H        ;Status Port
                DATA        EQU         0F0H        ;Data Port
                IBMASK      EQU         02H         ;IBF Mask

            CSEG

DACOFF:         OUT         STATUS                  ;Software Reset
                MVI         B, 0BH                  ;Select number of channels to scan
                CALL        OUTRDY                  ;Output when UPI ready

                MVI         B, 0                    ;Select channel 0,
                CALL        OUTRDY                  ;Output LOW BYTE data = 0
                CALL        OUTRDY                  ;Output HIGH BYTE data = 0
                RET

OUTRDY:         IN          STATUS                  ;Read status byte
                ANI         IBMASK                  ;Check for IBF = 1
                JNZ         OUTRDY                  ;Yes, check again
                MOV         A, B                    ;No, prepare data
                OUT         DATA                    ;Send data
                RET
```